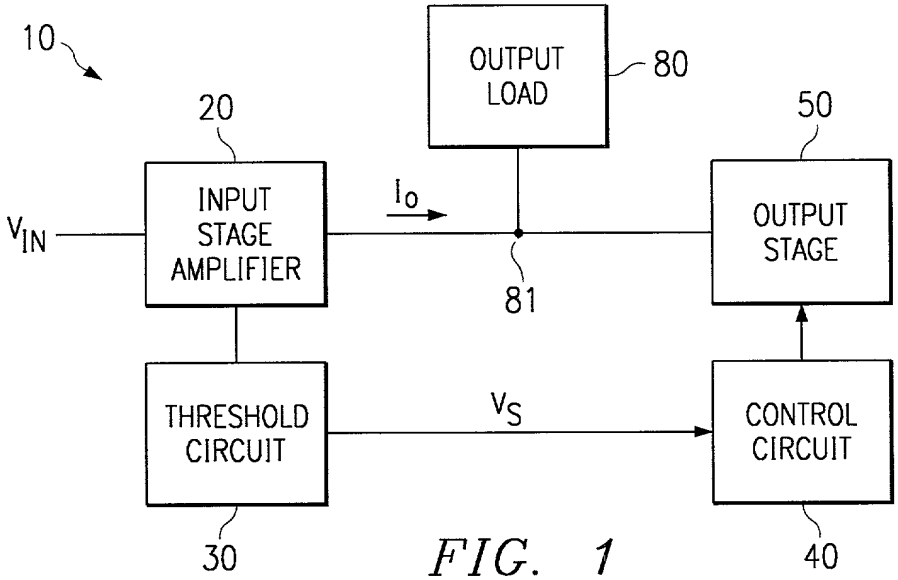
10
OUTPUT LOAD
80
20
50
INPUT STAGE AMPLIFIER
I_O
V_{IN}
OUTPUT STAGE
81
THRESHOLD CIRCUIT
V_S
CONTROL CIRCUIT
30
40

FIG. 1

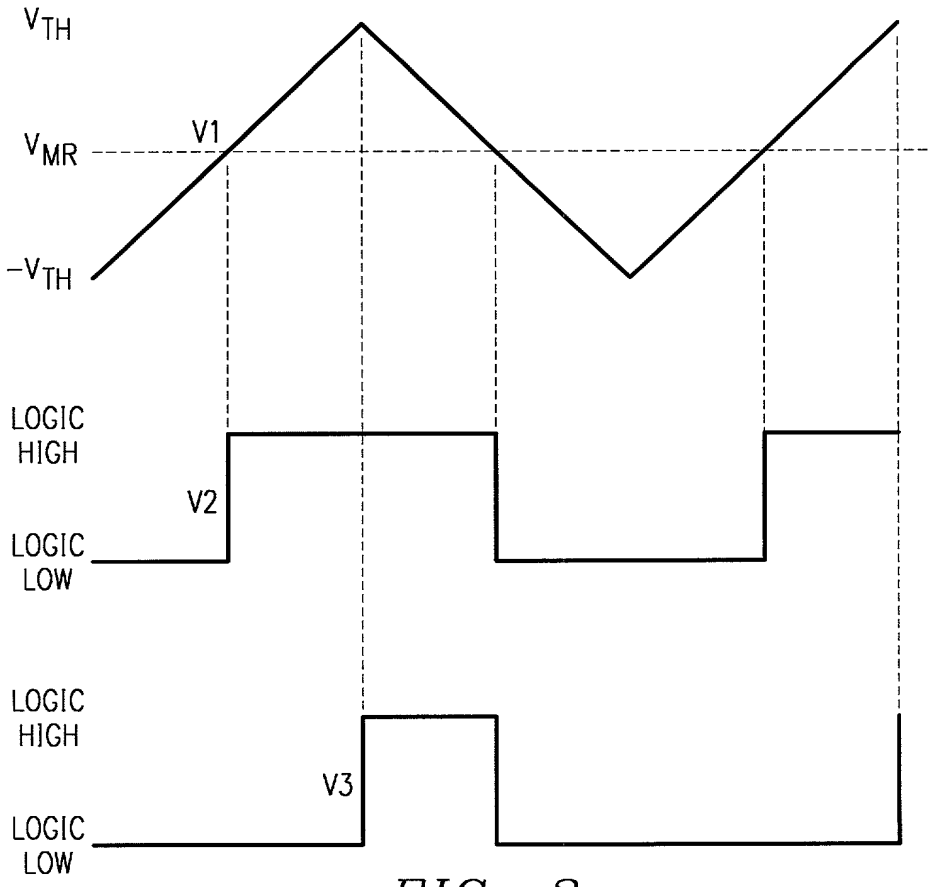
V_{TH}
V_{MR}
V1
$-V_{TH}$
LOGIC HIGH
V2
LOGIC LOW
LOGIC HIGH
V3
LOGIC LOW

FIG. 3

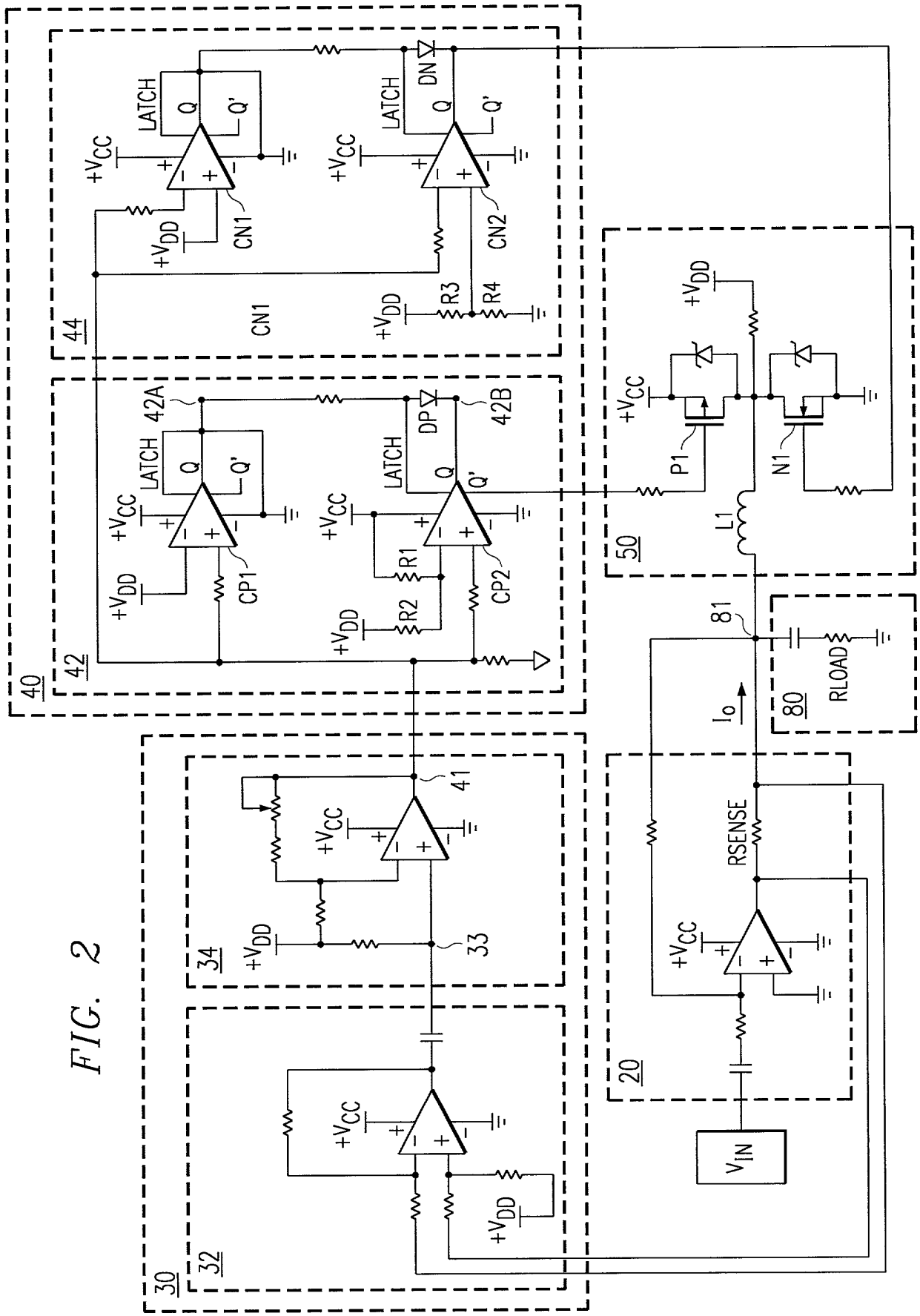
40
42
44
LATCH
Q
Q'
+VCC
+VDD
CN1
CN2
DN
DP
42A
42B
CP1
CP2
R1
R2
R3
R4
50
P1
N1
L1
81
80
RLOAD
Io
20
RSENSE
VIN
30
32
34
41
33

FIG. 2